Lab 7: Lab Report

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Abstract

Slow Clock:

The typical slow clock process

Register:

The typical register process where Q take D on load

ALU:

A multiplexer where the ALU selector bits chooses which operation is pushed to the output

BusMux:

A multiplexer that can pass the 8 bit value of X, the 8 bit value of Y, 0 or the output from the ALU.

Seg7Decode:

Given the DispSel bits and the output of register B, the seg7decoder will display *spCon, ready,* or the value of the calculation.

Controller:

Handles the logic behind on how to calculate the answer for the four functions.

Circuit

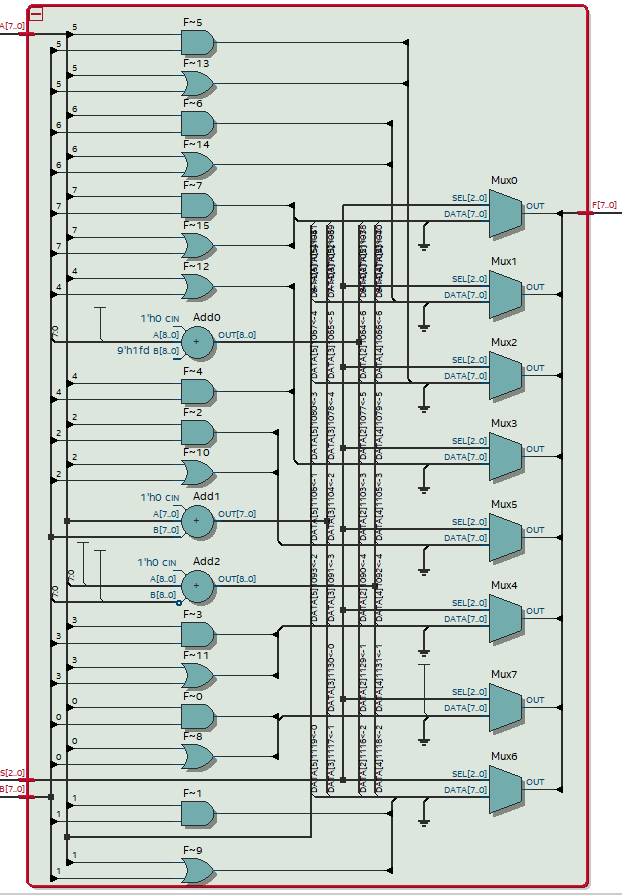


Figure : ALU

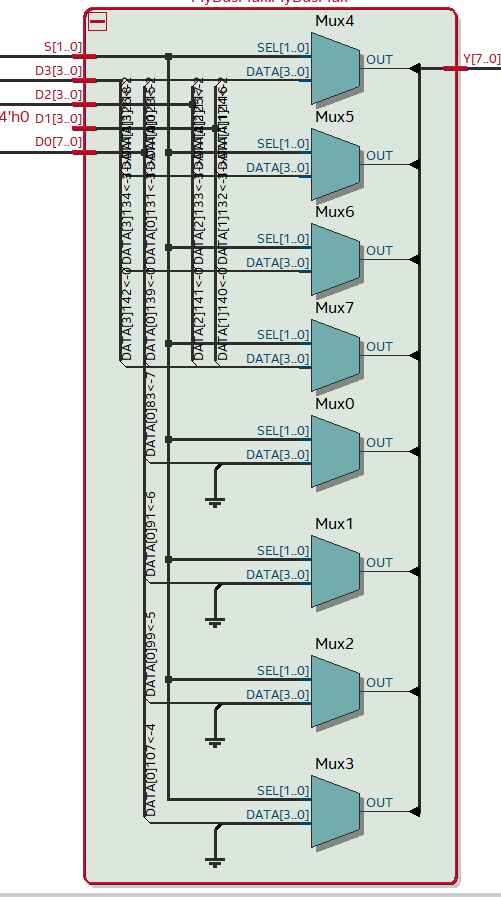


Figure : MyBusMux

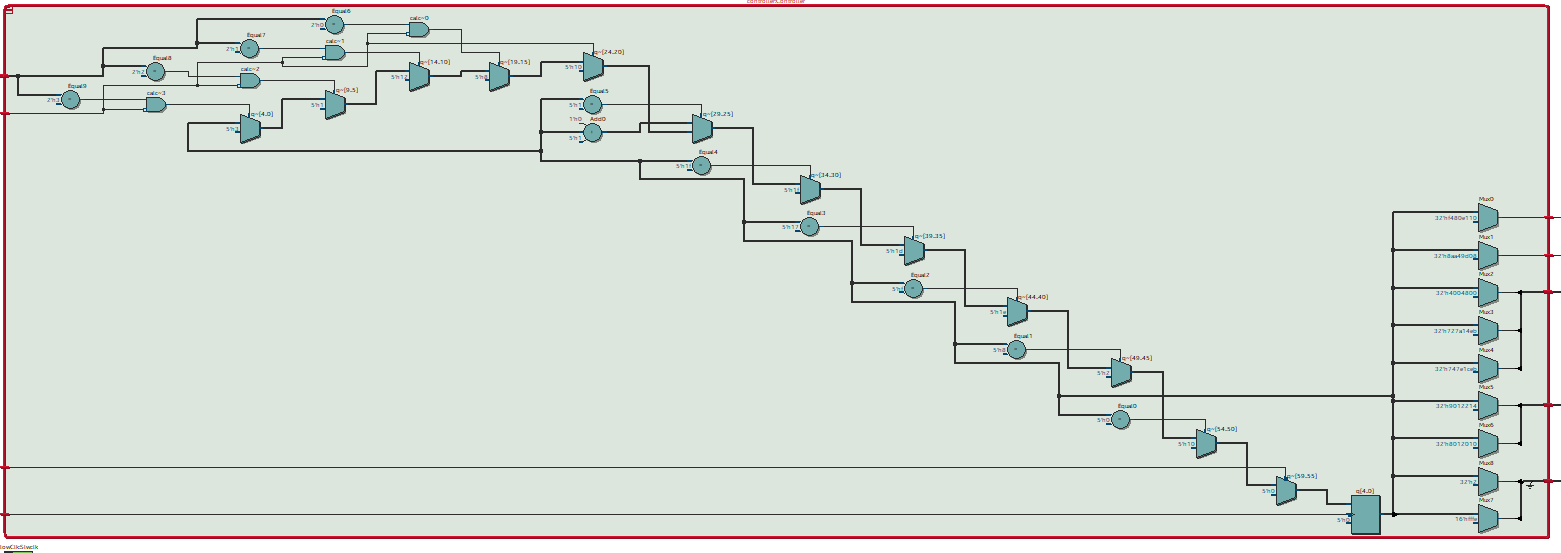


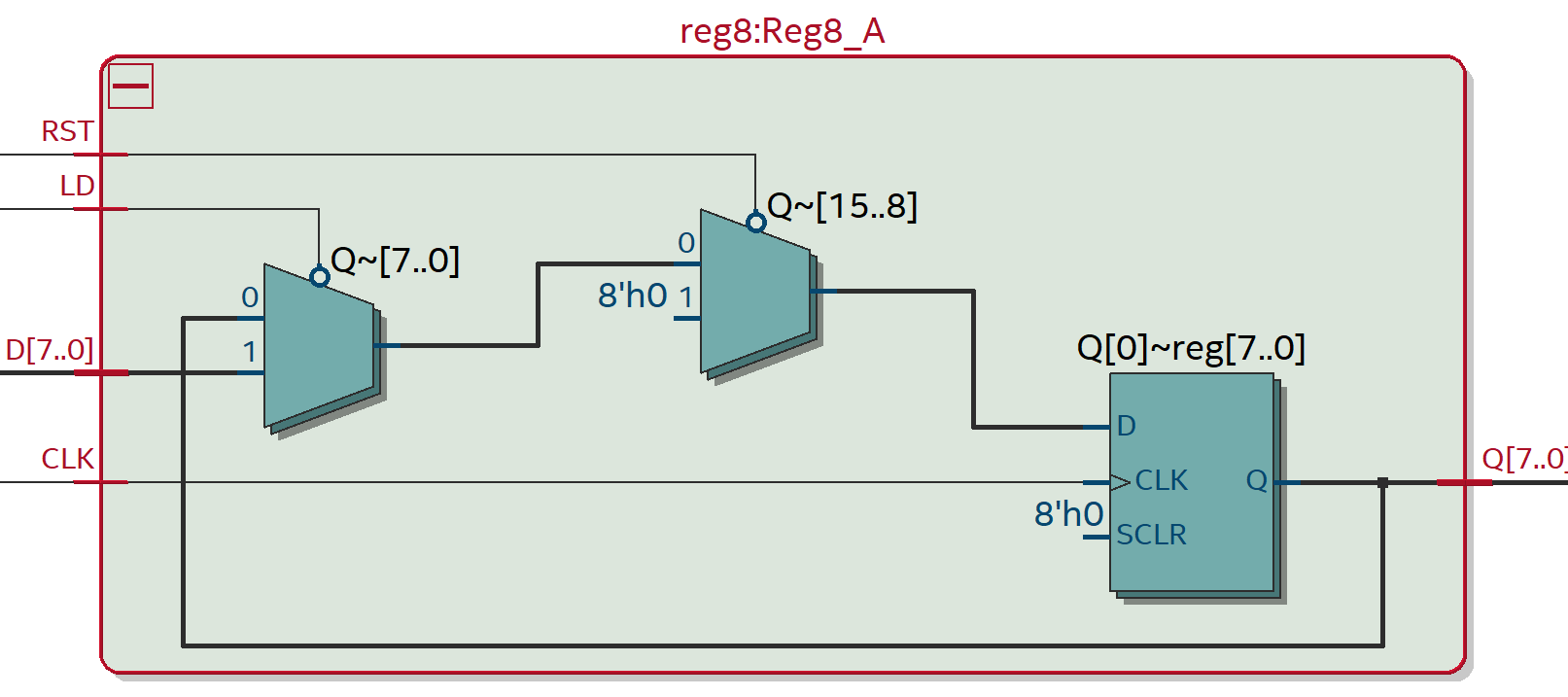
Figure : Controller

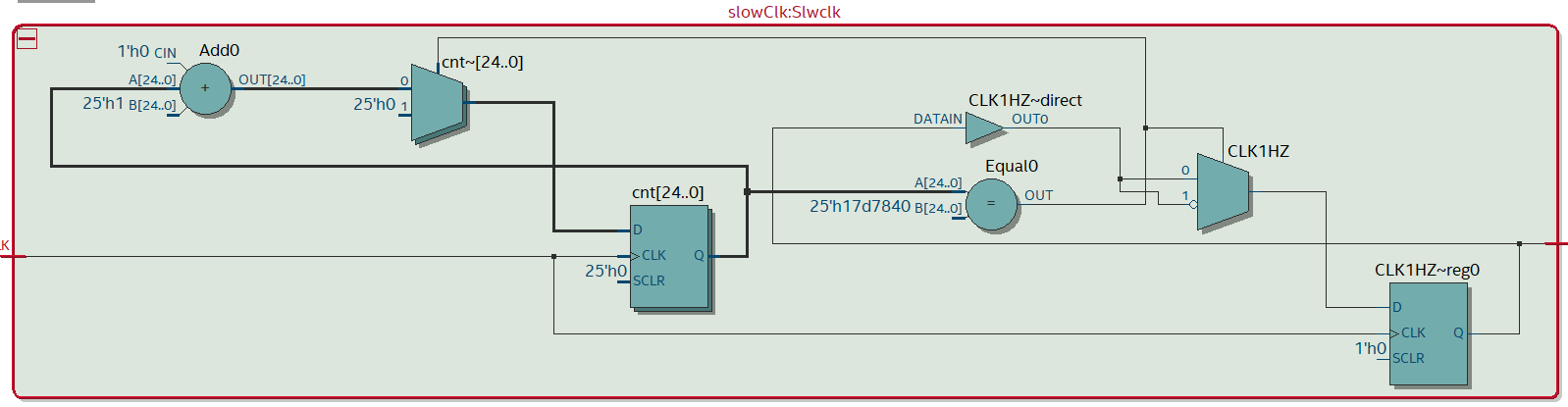
Figure : register

Figure : Slow Clock

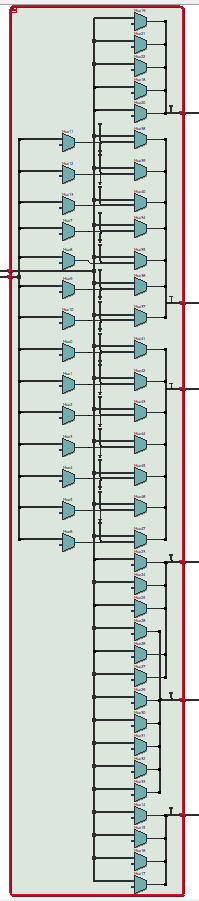


Figure :Seg7Decode

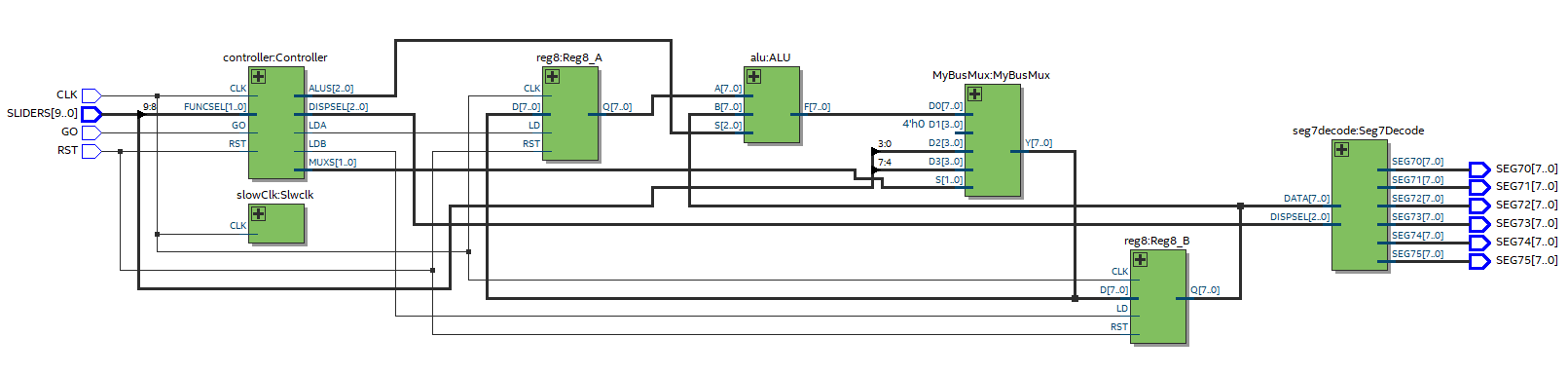


Figure : top level entity

Simulations

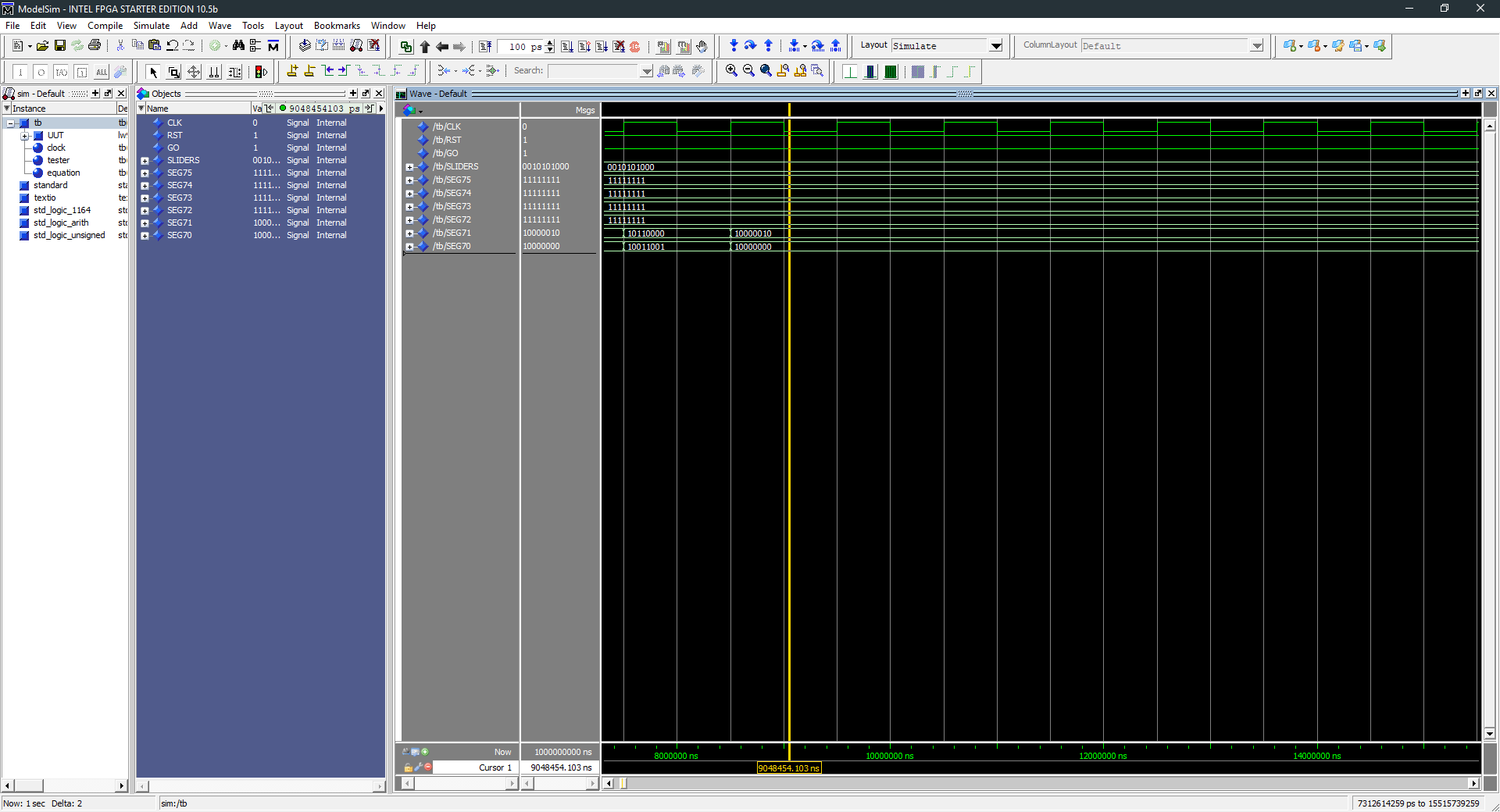


Figure : function 0

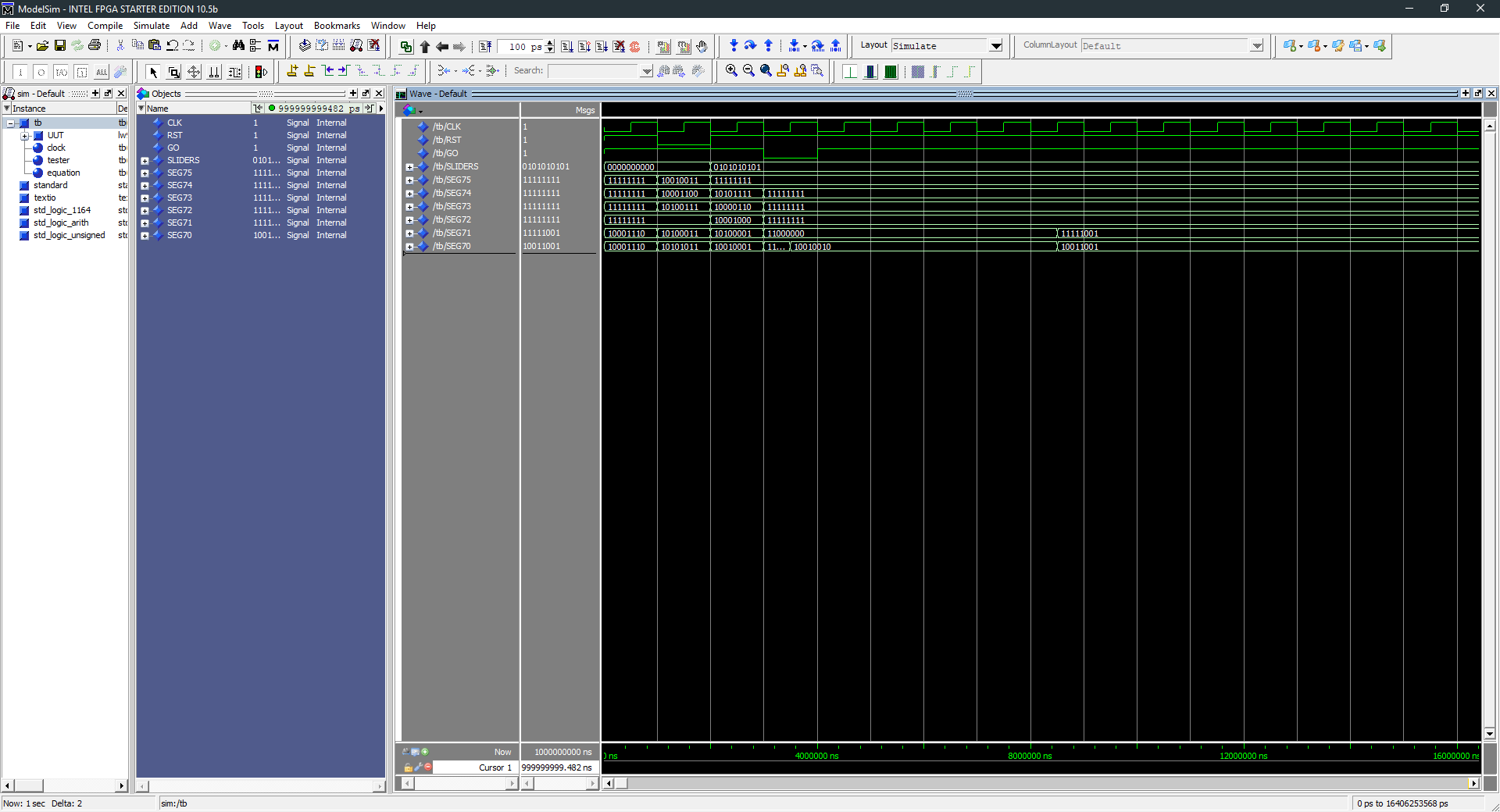


Figure : function 1

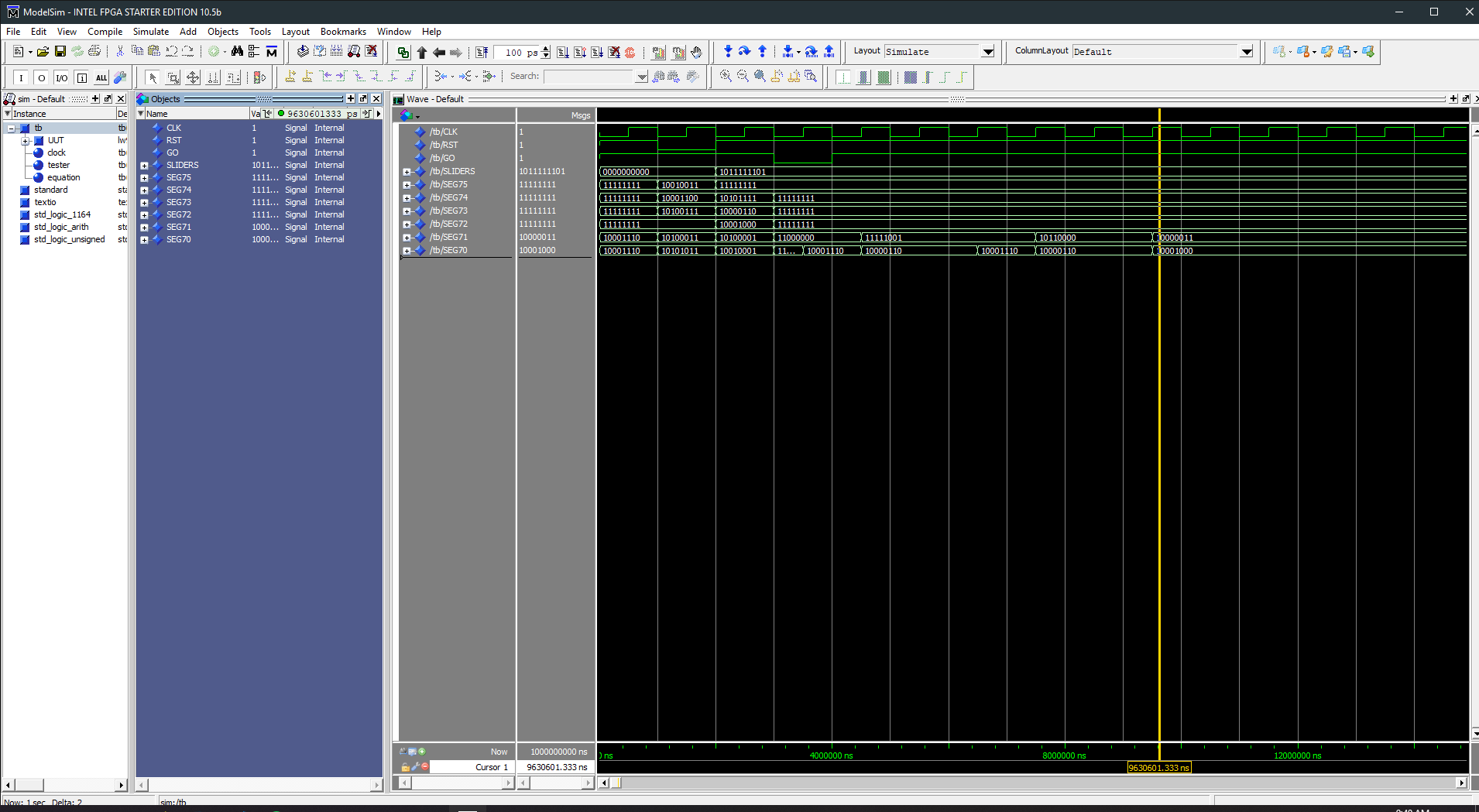


Figure : function 2

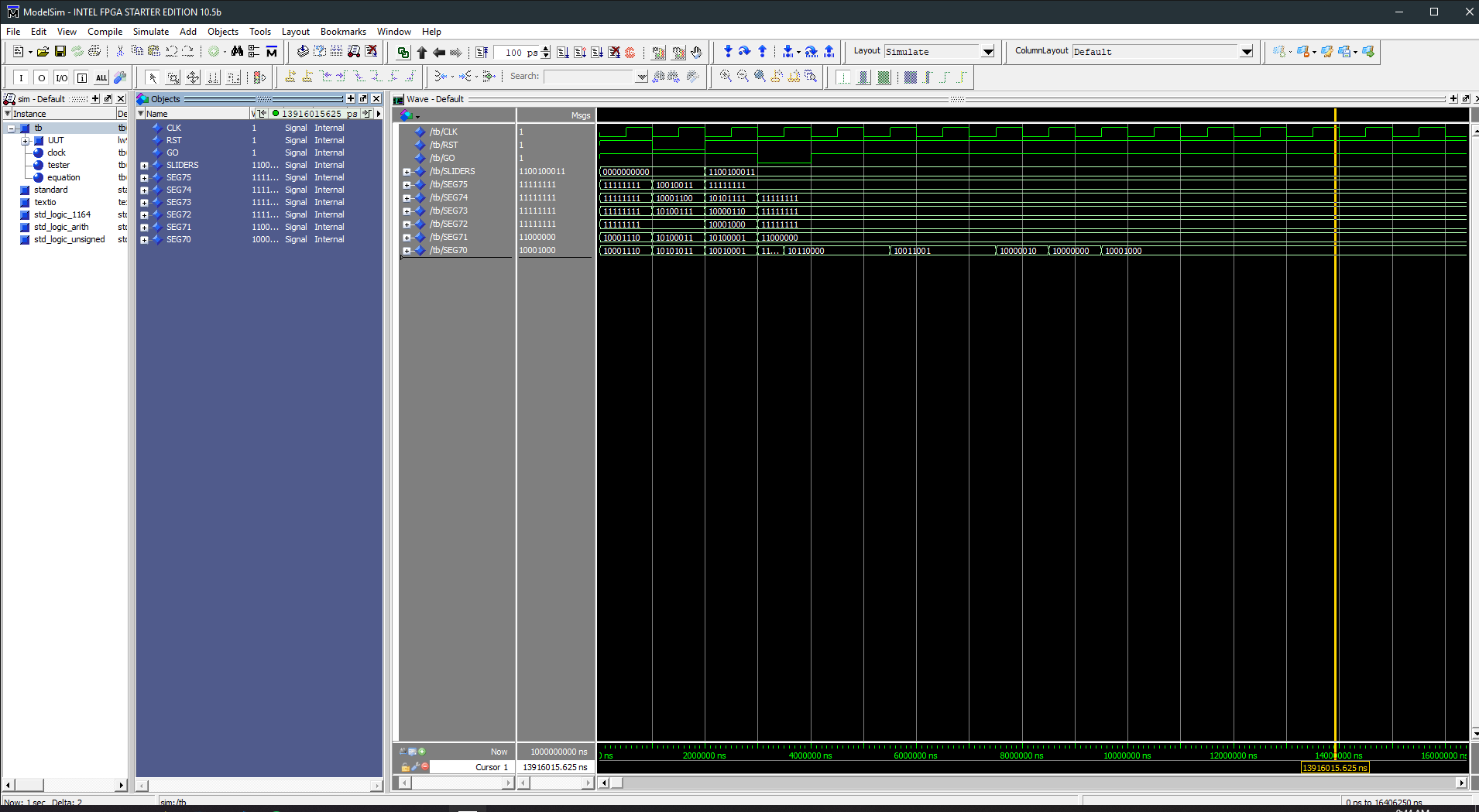


Figure : 3

Conclusion

I learned how complicated and complex it can be to do relatively simple calculations .